CLAIMS

1. A method for testing a fixed logic device formed within a gasket, comprising:

receiving an FPGA scan chain and configuring an FPGA fabric portion for a specified test;

producing a test signal to the fixed logic device;

receiving an output test signal from the fixed logic device;

applying a signature function to the received output test signal;

repeating the producing, receiving and applying steps for a specified number of times; and

determining if a value of the signature function corresponds to an expected value.

2. The method of claim 1 further comprising the step of isolating the fixed logic device that is to be tested.

3. The method of claim 1 further comprising the step of transmitting a test signal to the fixed logic device by way of an isolation circuit element.

4. The method of claim 1 further comprising the step of receiving an output test signal from the fixed logic device by way of an isolation circuit element.

5. The method of claim 1 wherein the determining step is performed by logic within an FPGA fabric portion.

6. The method of claim 1 wherein the determining step is performed by an external tester.

7. The method of claim 1 wherein the determining step includes the step of comparing the signature to an expected value.

8. An FPGA, comprising:

an FPGA fabric portion;

a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion; and

isolation circuitry formed within the Gasket, the isolation circuitry being serially coupled to receive test signals from the FPGA fabric portion.

9. The FPGA of claim 8 wherein the isolation circuitry includes a multiplexer array, which multiplexer array facilitates sending test signals directly to a device under test.

10. The FPGA of claim 8 wherein the isolation circuitry includes a multiplexer array, which multiplexer array facilitates sending test signal outputs directly from a device under test to the FPGA fabric.

11. An FPGA, comprising:

an FPGA fabric portion;

a Gasket formed at least partially within the FPGA fabric portion, the Gasket forming interfacing logic between an embedded core device and the fabric portion;

at least one multiplexer; and

a fixed logic device formed within the Gasket, the fixed logic device being coupled between the multiplexer and the FPGA fabric portion.

12. The FPGA of claim 11 wherein the multiplexer is coupled to receive outputs from the fixed logic device.

13. The FPGA of claim 12 wherein the multiplexer is coupled to receive test signals from the FPGA fabric portion by way of communication paths formed within the Gasket portion, which communication paths are accessible while the FPGA is configured for testing at least a portion of the

Gasket.

14. The FPGA of claim 13 wherein the multiplexer couples the test signals received from the FPGA fabric portion to the fixed logic device whenever the FPGA is configured for testing at least a portion of the Gasket.

15. The FPGA of claim 11 wherein the multiplexer is coupled to receive outputs from an embedded core device and to produce the received outputs to the fixed logic device whenever the FPGA fabric portion is not configured to test at least a portion of the Gasket.

16. An array of isolation circuit elements formed within a Gasket surrounding an embedded fixed logic core device, all within an FPGA, comprising:

at least one isolation circuit element configured for isolating the embedded fixed logic core device; and

at least one isolation circuit element configured for isolating a fixed logic device formed within the Gasket.

17. The array of claim 16 being coupled to receive outputs from the embedded fixed logic core device and to produce the outputs to one of a fixed logic device or to a fabric portion of the FPGA.

18. The array of claim 16 being coupled to receive outputs from the fixed logic device and test signals from a fabric portion of the FPGA and to produce the received signals to an embedded fixed logic core device according to whether the FPGA is configured for performing test or for routine operations.

19. An FPGA, comprising:

ID circuitry for delivering a device ID to an embedded device;

input circuitry for receiving test signals from test

circuitry; and

multiplexer circuitry coupled to receive input test signals and control signals from the input circuitry and ID information from the ID circuitry, and to produce selected input signals to the embedded device.

20. The FPGA of claim 19 further comprising test circuitry coupled to the input circuitry to produce test and control signals thereto.

21. The FPGA of claim 19 being configurable to connect the input circuitry to pins that may be connected to external test equipment, which external test equipment is for producing test signals that are received by the multiplexer circuitry and conducted to the inputs of the embedded device.

22. An FPGA configured in a test mode of operation, comprising:

first logic circuitry forming a plurality of latches for receiving an FPGA scan chain containing test vectors;

second logic circuitry forming a test output signature generator;

third logic circuitry configured for performing a specified test; and

fourth logic circuitry for determining whether the FPGA passed or failed a test.

23. The FPGA of claim 22 wherein each of the first, second and third logic circuitry are formed to communication with a fixed logic device within an FPGA Gasket.

24. The FPGA of claim 23 wherein the fixed logic device is formed within the Gasket.

25. The FPGA of claim 23 wherein the fixed logic device is an embedded core processor that is embedded within the Gasket.

26. An FPGA, comprising:

an FPGA fabric portion;

a gasket forming an interfacing logic portion between an embedded device and the FPGA fabric portion;

a first communication path in the gasket that directly couples at least one pin of the embedded device to the FPGA fabric portion; and

a second communication path in the gasket that directly couples the FPGA fabric portion to test circuitry formed within the gasket, which test circuitry further is coupled to at least one pin of the embedded device.

27. The FPGA of claim 26 wherein the test circuitry couples the FPGA fabric portion to at least one pin of the embedded device whenever the FPGA is configured to test the embedded device.

28. The FPGA of claim 26 wherein the first communication path is for conducting at least one device scan chain to the embedded core device.

29. An FPGA, comprising:

an FPGA fabric portion;

a gasket forming an interfacing logic portion between an embedded device and the FPGA fabric portion;

a first communication path in the gasket that directly couples the FPGA fabric portion to test circuitry formed within the gasket;

a second communication path in the gasket that directly couples at least one pin of an embedded device to the test circuitry; and

a third communication path in the gasket that couples an output of the test circuitry to an input of a fixed logic device formed within the gasket.

30. The FPGA of claim 29 wherein the test circuitry couples the FPGA fabric portion to the input of the fixed

logic device whenever the FPGA is configured to test the fixed logic device.

31. The FPGA of claim 29 wherein the first communication path is for conducting at least one device scan chain to the embedded core device.

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